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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
09/235,770	01/25/99	YAMAZAKI S	0756-1914

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SCHILLINGER,L	
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SIXBEY FRIEDMAN LEEDOM & FERGUSON
2010 CORPORATE RIDGE
SUITE 600
MCLEAN VA 22102

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Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary

Application No.	Applicant(s)
09/235,770	Yamazaki et al
Examiner	**Group Art Unit**
Laura Schillinger	2813

☒ Responsive to communication(s) filed on *Jan 25, 1999*

☐ This action is **FINAL.**

☐ Since this application is in condition for allowance except for formal matters, **prosecution as to the merits is closed** in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

A shortened statutory period for response to this action is set to expire *3* month(s), or thirty days, whichever is longer, from the mailing date of this communication. Failure to respond within the period for response will cause the application to become abandoned. (35 U.S.C. § 133). Extensions of time may be obtained under the provisions of 37 CFR 1.136(a).

Disposition of Claim

☒ Claim(s) *1-22* is/are pending in the applicat

Of the above, claim(s) _____ is/are withdrawn from consideration

☐ Claim(s) _____ is/are allowed.

☒ Claim(s) *1-22* is/are rejected.

☐ Claim(s) _____ is/are objected to.

☐ Claims _____ are subject to restriction or election requirement.

Application Papers

☐ See the attached Notice of Draftsperson's Patent Drawing Review, PTO-948.

☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

☐ The proposed drawing correction, filed on _____ is ☐ approved ☐ disapproved.

☐ The specification is objected to by the Examiner.

☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

☒ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

☒ All ☐ Some* ☒ None of the CERTIFIED copies of the priority documents have been

☐ received.

☒ received in Application No. (Series Code/Serial Number) *08/841,638* .

☐ received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

*Certified copies not received: _____

☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

☒ Notice of References Cited, PTO-892

☐ Information Disclosure Statement(s), PTO-1449, Paper No(s). _____

☐ Interview Summary, PTO-413

☐ Notice of Draftsperson's Patent Drawing Review, PTO-948

☐ Notice of Informal Patent Application, PTO-152

--- SEE OFFICE ACTION ON THE FOLLOWING PAGES ---

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-2, 4-5, 7-8, 10-12, 14-15, 17-18, and 20-22 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Wakai ('230).

In reference to claim 1, Wakai teaches a device comprising:

a first layer of SiN formed on a substrate (Fig 9 (1a) and Col.5, lines:1-5);

a layer of SiO formed on the SiN layer (Fig 9 (1a) and Col.5, lines:1-5);

a semiconductor layer formed on the SiO layer, having a source, drain and channel (Fig.9 (6));

another SiO layer and SiN layer on top of the semiconductor layer, (Fig.9 (7) and Col.4, lines: 1-10) and a gate (Fig.9 (8)).

In reference to claim 2, Wakai teaches wherein the top SiN layer is doped with H and O (Col.4, lines: 10-20).

In reference to claim 4, Wakai teaches a device comprising:

a first layer of SiN formed on a substrate (Fig 9 (1a) and Col.5, lines:1-5);

a layer of SiO formed on the SiN layer (Fig 9 (1a) and Col.5, lines:1-5);

a semiconductor layer formed on the SiO layer, having a source, drain and channel (Fig 9 (6));

another SiO layer which extends the beyond the edges of the semiconductor layer (Fig.9 (7) and Col.4, lines: 1-10);

a second SiN layer which extends the beyond the edges of the semiconductor layer (Fig.9 (7) and Col.4, lines: 1-10);

and a gate electrode formed over a channel (Fig.9 (8)).

In reference to claim 5, Wakai teaches wherein the second SiN film is doped with H and O (Col.4, lines:10-20) .

In reference to claim 7, Wakai teaches a device comprising:

a first layer of SiN formed on a substrate (Fig 9 (1a) and Col.5, lines:1-5);

a layer of SiO formed on the SiN layer (Fig 9 (1a) and Col.5, lines:1-5);

a semiconductor layer formed on the SiO layer, having a source, drain and channel (Fig 9 (6));

another SiO layer which extends the beyond the edges of the semiconductor layer (Fig.9 (7) and Col.4, lines: 1-10);

a second SiN layer which extends the beyond the edges of the semiconductor layer (Fig.9 (7) and Col.4, lines: 1-10);

and a gate electrode formed over a channel (Fig.9 (8));

wherein the source and drain regions are doped with H (Col.4, lines: 10-25).

In reference to claim 8, Wakai teaches wherein the SiN layer is doped with H or O (Col.4, lines: 10-25).

In reference to claim 10, Wakai teaches a device comprising:

a substrate (Fig.9 (1));

a first layer of SiN formed on a substrate (Fig 9 (1a) and Col.5, lines:1-5);

a layer of SiO formed on the SiN layer (Fig 9 (1a) and Col.5, lines:1-5);

a semiconductor layer formed on the SiO layer, having a source, drain and channel (Fig 9 (6));

another SiO layer which extends the beyond the edges of the semiconductor layer (Fig.9 (7) and Col.4, lines: 1-10);

a second SiN layer which extends the beyond the edges of the semiconductor layer (Fig.9 (7) and Col.4, lines: 1-10);

and a gate electrode formed over a channel (Fig.9 (8)).

In reference to claim 11, Wakai teaches wherein the second SiN film is doped with H or O (Col.4, lines: 10-25).

In reference to claim 12, Wakai teaches a device comprising:

a first layer of SiN formed on a substrate (Fig 9 (1a) and Col.5, lines:1-5);

a layer of SiO formed on the SiN layer (Fig 9 (1a) and Col.5, lines:1-5);

a semiconductor layer formed on the SiO layer, having a source, drain and channel (Fig.9 (6));

another SiO layer which extends the beyond the edges of the semiconductor layer (Fig.9 (7) and Col.4, lines: 1-10);

a second SiN layer which extends the beyond the edges of the semiconductor layer (Fig.9 (7) and Col.4, lines: 1-10);

wherein the source and drain regions are doped with H (Col.4, lines: 10-25).

In reference to claim 14, Wakai teaches wherein the gate electrode is adjacent to the channel (Fig.9 (8)).

In reference to claim 15, Wakai teaches a device comprising:

a first layer of SiN formed on a substrate (Fig 9 (1a) and Col.5, lines:1-5);

a layer of SiO formed on the SiN layer (Fig 9 (1a) and Col.5, lines:1-5);

a semiconductor layer formed on the SiO layer, having a source, drain and channel (Fig.9 (6));

another SiO layer which extends the beyond the edges of the semiconductor layer (Fig.9 (7) and Col.4, lines: 1-10);

a second SiN layer which extends the beyond the edges of the semiconductor layer (Fig.9 (7) and Col.4, lines: 1-10);

wherein both SiN layers are formed between the first and second TFTs (Fig.9 (7) and Col.4, lines: 1-10).

In reference to claim 17, Wakai teaches further comprising a gate electrode adjacent to the channel (Fig.9 (8)).

In reference to claim 18, Wakai teaches a device comprising:

a first layer of SiN formed on a substrate (Fig 9 (1a) and Col.5, lines:1-5);

a layer of SiO formed on the SiN layer (Fig 9 (1a) and Col.5, lines:1-5);

a semiconductor layer formed on the SiO layer, having a source, drain and channel (Fig.9 (6);

another SiO layer which extends the beyond the edges of the semiconductor layer (Fig.9 (7) and Col.4, lines: 1-10);

a second SiN layer which extends the beyond the edges of the semiconductor layer (Fig.9 (7) and Col.4, lines: 1-10);

a gate electrode formed over the channel region (Fig.9 (8));

at least one electrode formed on the interlayer insulating film wherein at least one electrode is connected to one of the source and drain regions via a contact hole through the interlayer insulating film and upper two insulating films (Fig.9 (11)).

In reference to claim 20, Wakai teaches a device comprising:

a first layer of SiN formed on a substrate (Fig 9 (1a) and Col.5, lines:1-5);

a layer of SiO formed on the SiN layer (Fig 9 (1a) and Col.5, lines:1-5);

a semiconductor layer formed on the SiO layer, having a source, drain and channel (Fig.9 (6));

another SiO layer which extends the beyond the edges of the semiconductor layer (Fig.9 (7) and Col.4, lines: 1-10);;

a second SiN layer which extends the beyond the edges of the semiconductor layer (Fig.9 (7) and Col.4, lines: 1-10);;

a gate electrode formed over the channel region (Fig. 9 (8));

at least one electrode formed on the interlayer insulating film wherein at least one electrode is connected to one of the source and drain regions via a contact hole through the interlayer insulating film and upper two insulating films (Fig.9 (11)).

In reference to claim 21, Wakai teaches wherein the semiconductor is crystalline Si (Col.3, lines: 45-50).

In reference to claim 22, Wakai teaches wherein the substrate is glass (Col.2, lines: 60-65).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 3, 6, 9, 13, 16, 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wakai ('230).

In reference to claims 3, 6, 9, 13, 16, 19 applicant claims wherein the first SiN layer is 10-50 nm and the first SiO layer is 10-800 nm, and the second SiO layer is 50-200 nm, and the second SiN

layer is 2-20 nm. Wakai teaches all of the above device components however fails to explicitly teach their thicknesses.

However, these claims are prima facie obvious without showing that the claimed ranges achieve unexpected results relative to the prior art range. In re Woodruff, 16 USPQ2d 1935, 1937 (Fed. Cir. 1990). See also In re Huang, 40 USPQ2d 1685, 1688(Fed. Cir. 1996)(claimed ranges of a result effective variable, which do not overlap the prior art ranges, are unpatentable unless they produce a new and unexpected result which is different in kind and not merely in degree from the results of the prior art). See also In re Boesch, 205 USPQ 215 (CCPA) (discovery of optimum value of result effective variable in known process is ordinarily within skill of art) and In re Aller, 105 USPQ 233 (CCPA 1955) (selection of optimum ranges within prior art general conditions is obvious).

Conclusion

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Liaw ('249) teaches a similar device for a SRAM. Zhou et al ('627) teaches a similar structure form a MOSFET.

6. Any inquiry concerning this communication from examiner should be directed to Laura Schillinger whose telephone number is (703) 308-6425. The examiner can normally be reached by telephone on Monday to Friday from 6:30 AM to 4:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Charles Bowers, can be reached on (703) 308-2417. The fax phone number for the group is (703) 308-7722.

LMS

Charles Bowers
Supervisory Patent Examiner
Technology Center 2800

August 31, 2000